# KWIK CIRCUIT FAQ

## SPICE Model for a Platinum RTD Sensor

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## FAQ: How to model a platinum RTD sensor in SPICE

### Introduction / Overview

A KWIK (Know-how With Integrated Knowledge) Circuit application note provides a step-by-step guide to addressing a specific design challenge. For a given set of application circuit requirements, it illustrates how these are addressed using generic formulae and makes them easily scalable to other similar application specifications. This sensor model enables SPICE simulation of the electrical and physical properties of a Resistance Temperature Detector (RTD). The SPICE model uses parameters which characterize the physical behavior of an RTD which translates temperature into electrical resistance. It also provides a typical excitation and signal conditioning circuit that can be used to demonstrate the behavior of the RTD model.

### RTD Overview

RTDs are resistive elements whose resistance changes in response to a change in temperature. Since their behavior is well understood, they can be used to make precision temperature measurements, with an accuracy of under 0.1°C. RTDs are typically constructed from a length of wire wrapped around a ceramic or glass core but they can also be constructed from thick film resistors plated onto a substrate. The resistive wire used is

typically platinum but may also be either nickel or copper. The PT100 is a common RTD constructed from platinum with a resistance of 100 Ω at 0°C. RTD elements are also available with 0°C resistances of 200, 500, 1000, and 2000 Ω. The relationship between platinum RTD resistance and temperature is described by the Callendar-Van Dusen (CVD) equation. Equation 1 describes RTD resistance for temperatures below 0°C while Equation 2 describes RTD resistance for temperatures above 0°C for a PT100 RTD.

For T < 0:

$$R(T) = R0 \cdot \{1 + (A \cdot T) + (B \cdot T2) + [(C \cdot T3) \cdot (T - 100)]\} \quad (1)$$

For T > 0:

$$R(T) = R0 \cdot [1 + (A \cdot T) + (B \cdot T2)]$$

The coefficients in the Callendar-Van Dusen equations are defined by the IEC-60751 standard. R0 is the resistance of the RTD at 0°C. For a PT100 RTD, R0 is 100 Ω. For IEC 60751 standard PT100 RTDs, the coefficients are:

$A = 3.9083 \cdot 10\text{-}3$

$B = -5.775 \cdot 10\text{-}7$

$C = -4.183 \cdot 10\text{-}12$

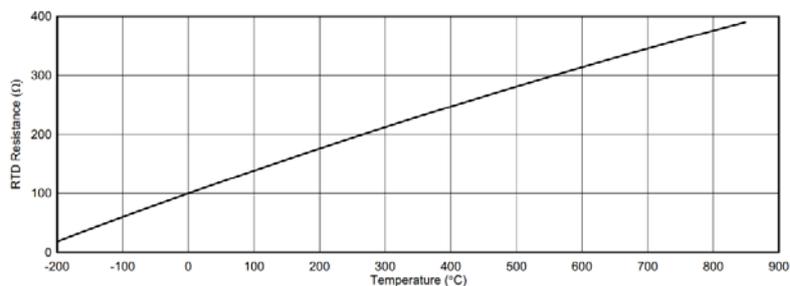The change in resistance from -200 °C to 850 °C of a PT100 RTD is shown in Figure 1.



*Figure 1. PT100 RTD Resistance From −200°C to 850°C*

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## Design Descriptions

This RTD Model ( Figure 2) is simulated using LTSPICE but is also PSPICE compatible. The model enables users to simulate sensor loading of a reference excitation current and to connect signal conditioning circuitry to the RTD. This enables simulation of all common mode, differential, and source impedance effects. The model assumes that RTD resistance changes in response to temperature. Only nominal sensor specifications are modeled. T1 is the parameter used by the model to denote temperature in the equations that describe RTD behavior. This is separate to temp, the variable used in SPICE for global temperature. This approach enables the model to demonstrate the behavior of the RTD only, without affecting the performance of other components in the circuit.

## Design Tips / Considerations

1. Excite the sensor model using a current source which allows the RTD resistance to be measured as a voltage.

2. Connect the RTD sensor output to any high input impedance signal conditioning circuitry being used for common mode, differential, full range, and accuracy simulations.

3. Use SPICE parameter stepping (. step param) with a DC Analysis (. op) to sweep from minimum to maximum temperature applied to the sensor model.

## Design Procedure

1. Run a SPICE simulation (using the sweep parameter) and confirm that the RTD output voltage matches the expected output for a given temperature. Note that Vrtd = (Vrtd+) − (Vrtd-)

2. Connect the sensor model to an excitation current and signal conditioning circuit to simulate the complete application.

## Design Simulations

The simulation performs a sweep of RTD temperature from -200°C to 850°C using a 1mA excitation current. A table showing sample simulated versus calculated values (using the Callendar-Van Dusen equations) for RTD output voltage is shown in Table 1.

Table 1. Simulated versus ideal Results

| Temperature (°C) | RTD Output Voltage (mV) | Temperature (°C) |
|---|---|---|
| -200 | 18.520080 | 18.520080 |
| 0 | 100.000000 | 100.000000 |
| 850 | 390.481125 | 390.481125 |

```
.step param T1 -200 850 10
.param A=3.9083e-3
.param B=-5.775e-7
.param C=-4.183e-12
.param R0=100
.param UNIT=(IF(T1>0,1,0))
.param Rrtd=R0*(1+(A*T1)+(B*T1**2)+C*(T1-100)*(T1**3)*(1-UNIT))
.op
```
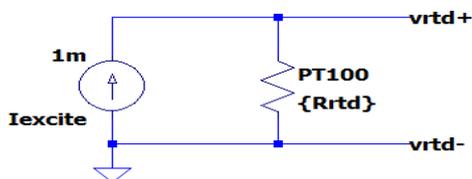


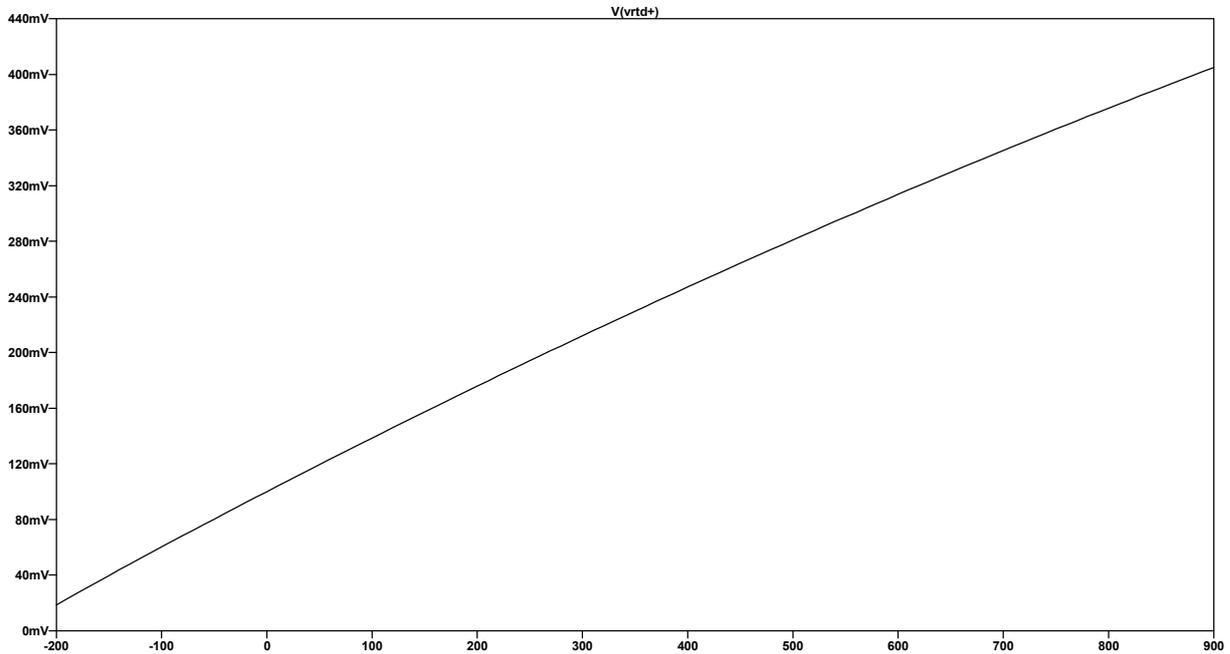Figure 2. Schematic showing RTD Model and Simulation Parameters

*Figure 3. Plot of simulated voltage versus temperature using PT100 SPICE RTD sensor mode and 1mA excitation*

A typical application circuit for the sensor model is shown in Figure 4. The value of Vc, which is generated by dividing down a 4.096V reference, is chosen to be within the DC common-mode range of the AD8538 op-amp to produce a 1mA (approx.) RTD excitation current when dropped across a high accuracy (0.1%) 3.01kΩ resistor. The high loop gain set by the AD8538 forces the excitation current through the RTD model to be:

$$Iexcite = \frac{Vc}{Rsense} = \frac{3.072V}{3.01k} = 1.0206mA$$

Two 499Ω resistors provide ESD protection for the input and output terminals of the AD8538 with 1nF capacitors for EMI and RFI filtering and a 2.2nF capacitor for loop stability. The RTD output voltage is conditioned using theAD8422 instrumentation amplifier whose gain is set to 9.959 by placing a 2.21kΩ resistor between its RG terminals. This value of gain is chosen to keep the output voltage of the AD8422 within the input range of an ADC also using a 4.096V voltage reference. The purpose of the resistors and capacitor at the input terminals of

the AD8422 is to provide differential and common-mode filtering from noise injected into cables in a real application. Resistor and capacitor values for gain and filtering were chosen from the datasheet for the AD8422. A plot of simulated output voltage versus temperature for the application circuit is shown in Figure 5. While this application circuit uses a model for a 2-wire RTD, it can be easily adapted to model a 3- or 4-wire RTD as shown in Figure 6. V1rtd and V4rtd are 0V voltage sources which are included in the schematic so that node labels do not conflict (SPICE simulation tools cannot accommodate two different node names having the same node). The 0V voltage sources have no effect on simulation results (behaving like a short-circuit) and help to present an RTD model that more closely emulates how RTD sensors are physically wired in a real-world application. Similarly, the models can be adapted for PT200, PT500, PT1000 and PT2000 RTDs by setting the setting the value of R0 in the schematic to be that of the required RTD (resistance at 0°C). Table 2 shows that the RTD voltage lies within the input

range required for linear operation of the AD8422 across the full temperature range and also that the overall output voltage of the application circuit lies within the input range of an ADC using a 4.096V reference voltage. Note that the LT1461 could be used to provide this reference voltage but was not included to simplify the schematic.

*Table 2. Simulated versus ideal Results*

| RTD Temperature, T1 (°C) | V (rtd+, rtd-) (mV) | Vout (V) |
|---|---|---|
| -200 | 18.520080 | 0.186543 |
| 0 | 100.000000 | 1.007521 |
| 850 | 390.481125 | 3.934359 |

```
.step param T1 -200 850 10
.param A=3.9083e-3
.param B=-5.775e-7
.param C=-4.183e-12
.param R0=100
.param UNIT = (IF(T1>0,1,0))
.param Rrtd=R0*(1+(A*T1)+(B*T1**2)+C*(T1-100)*(T1**3)*(1-UNIT))
.op
```
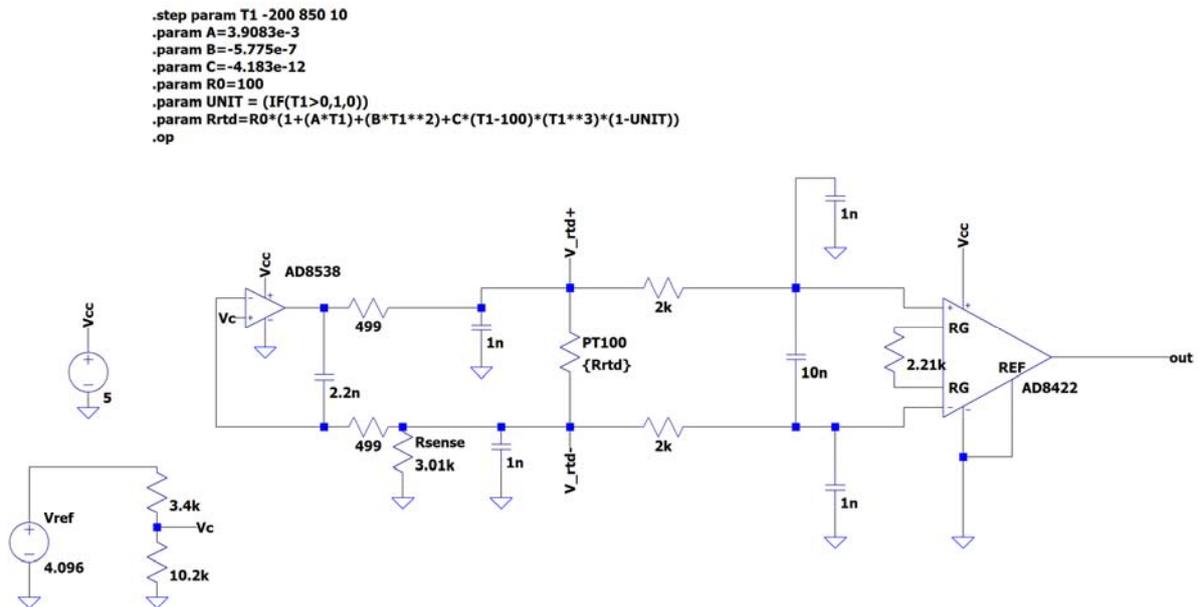


*Figure 4. PT100 2-wire RTD application circuit showing excitation and signal conditioning circuitry*
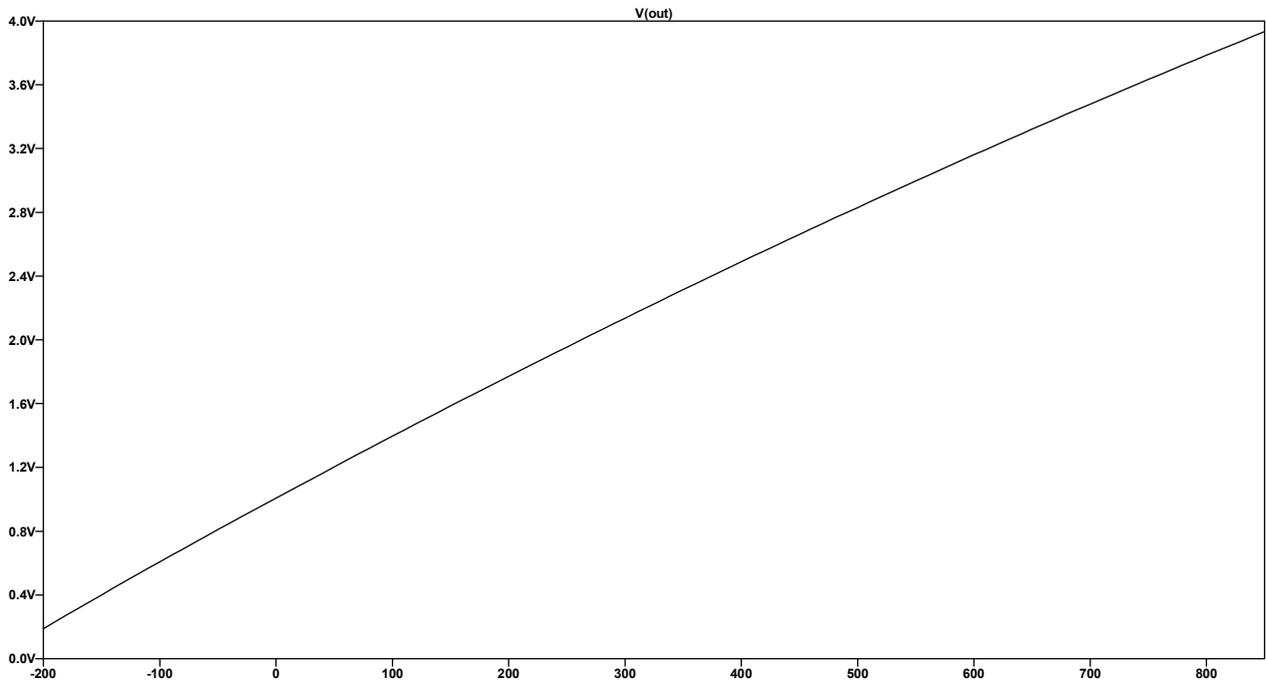
*Figure 5. Plot of simulated output voltage versus temperature for 2-wire RTD application circuit*
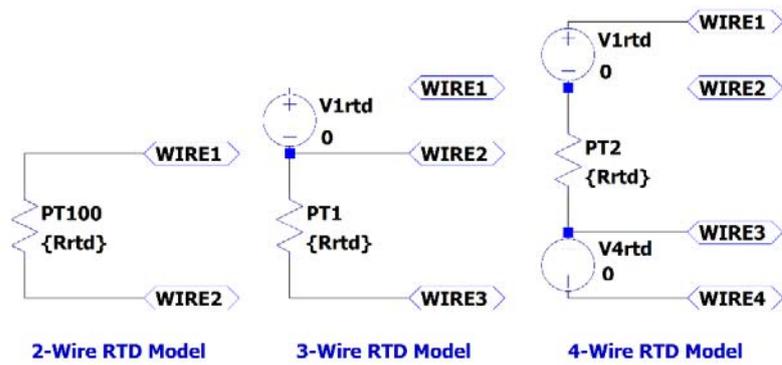


*Figure 6.  Adapting the 2-wire RTD model for 3- and 4-wire RTD applications*

## Design Devices

**Table 3. Series Voltage References**

| Part Number | Vout (V) typ | Initial Accuracy (%) max | Vout Tempco (ppm/V) max | Vnoise (Vp-p) typ | Iout Sourcing (A) max | Vs+ (V) min/max |
|---|---|---|---|---|---|---|
| LT1461ACS8-4 | 4.096 | 0.04 | 3 | 32u | 50m | 4.06/20 |

**Table 4. Instrumentation Amplifiers**

| Part Number | Vos (V) max | Ibias (A) max | Gain (V/V) min/max | BW Low Gain (Hz) typ | Vnoise (V/rt-Hz) typ | Vs span (V) min/max |
|---|---|---|---|---|---|---|
| AD8422 | 60u | 1n | 1/1000 | 2.2M | 8n | 4.6/36 |

**Table 5. Op Amps (for Reference & DAC Output Buffers, as needed)**

| Part Number | Vos (V) max | Ibias (A) max | GBP (Hz) typ | Vnoise (V/rt-Hz) typ | Iq/Amp (A) typ | Vs span (V) min/max |
|---|---|---|---|---|---|---|
| AD8538 | 13u | 25p | 430k | 50n | 180u | 2.7/5.0 |

## References

"Practical Design Techniques for Sensor Signal Conditioning"
Edited by Walt Kester, Analog Devices, 1999, ISBN-0-916550-20-6.
Education-library/practical-design-techniques-sensor-signal-conditioning.html

**Instrumentation Amplifier Diamond Plot Tool**
The Diamond Plot Tool is a web application that generates a configuration-specific Output Voltage Range vs. Input Common-Mode Voltage graph, also known as the Diamond Plot, for Analog Devices Instrumentation Amplifiers

LTSpice® is a high-performance SPICE III simulator, schematic capture and waveform viewer with enhancements and models for easing the simulation of switching regulator, linear, and signal chain circuits.

## Acknowledgments